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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/778,014	02/12/2004	Achim Gratz	10808/123	3343

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EXAMINER

SEFER, AHMED N

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

874

Office Action Summary	Application No. 10/778,014	Applicant(s) GRATZ ET AL.	
	Examiner A. Sefer	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2005.
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-72 is/are pending in the application.
 4a) Of the above claim(s) 52-72 is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 21-51 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 21-51) in the reply filed on 4/21/2005 is acknowledged.

Specification

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino

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acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

3. Claims 40, 45-47 are objected to because of the following informalities: The recitation, "... electrically insulting" of claim 40 should read "... electrically insulating" and the recitation, "the trench" of claims 45-47 should read "the at least one deep trench". Appropriate correction is required.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, **the plurality of deep trenches arranged next to one another in a transverse direction separating a plurality of charge storing layers/memory cells arranged in the transverse direction recited in claims 49 and 50 and the further at least one shallow trench -- which indicates additional shallow trench(s) -- recited in claim 37** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

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application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 41-43 and 36 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The application as originally filed does not specifically support the limitation of claim 41, "... the deep trench does not penetrate into the second charge storing layer". The specification merely discloses that the shallow trench does not penetrate through the charge storing layer (see page 6, lines 13-18).

The application as originally filed does not specifically support the limitation of claim 36, "at least one shallow trench having the same depth as the deep trench". The specification merely discloses that the shallow trench has a depth of less than 500 nm while the deep trench has a depth greater than 700 nm (see page 6, lines 1-10).

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

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The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 39 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 39 recites the limitation "the electrically conductive layer". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 21-29 and 45-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Gratz ("Gratz") US PG-Pub 2002/0024081.

Gratz discloses (fig. 3 and par. 0047) a semiconductor circuit arrangement on a substrate comprising: a doped semiconductor layer 3 having a first conductivity type disposed on the substrate; an insulating layer 8 disposed on the doped semiconductor layer; a charge storing layer 9 or a conducting layer (as in claim 22) or an insulating layer (as in claim 23) configured for storing an electrical charge disposed on the insulating layer; and at least one deep trench 5 that penetrates through the charge storing layer and extends into the doped semiconductor layer.

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Regarding claim 24, Gratz discloses at least one deep trench penetrating through the doped semiconductor layer into the substrate.

Regarding claim 25, Gratz discloses a second doped semiconductor layer 2 having a second conductivity type disposed between the substrate and the doped semiconductor layer, where the second conductivity type is opposite to the conductivity type of the doped semiconductor layer.

Regarding claim 26, Gratz discloses at least one deep trench penetrating through the doped semiconductor layer and extending into the second doped layer.

Regarding claim 27, Gratz discloses at least one deep trench penetrating through the doped semiconductor layer and the second semiconductor layer into the substrate.

Regarding claim 28, Gratz discloses a conductive layer 11 and a second insulating layer 10 where the second insulating layer is disposed on the charge storing layer and the conductive layer is disposed on the second insulating layer.

Regarding claim 29, Gratz discloses a shallow trench 5'' that is arranged in the doped semiconductor layer.

Regarding claims 45 and 46, Gratz discloses an insulating material 8/6 or silicon dioxide (as in claim 46) disposed on the wall of the trench.

Regarding claims 47 and 48, Gratz discloses the trench being filled with an electrically conductive or semi-conductive material or polysilicon (as in claim 48) and the material is isolated from the trench wall with the electrically insulating material.

11. Claims 21, 22, 25, 26, 28-32, 34, 35, 40-46 and 49-51 are rejected under 35 U.S.C. 102(e) as being anticipated by anticipated by Deml et al. ("Deml") US PG-Pub 2003/0075773.

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The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Deml discloses figs. 8 and 12-16 a semiconductor circuit arrangement forming a logic circuit arrangement (as in claim 35) on a substrate comprising: a doped semiconductor layer 220 having a first conductivity type disposed on the substrate; an insulating layer 230 disposed on the doped semiconductor layer; a charge storing layer 240 or a conducting layer (as in claim 22) configured for storing an electrical charge disposed on the insulating layer; and at least one deep trench 215 that penetrates through the charge storing layer and extends into the doped semiconductor layer.

Regarding claim 25, Deml discloses a second doped semiconductor layer 225 having a second conductivity type disposed between the substrate and the doped semiconductor layer, where the second conductivity type is opposite to the conductivity type of the doped semiconductor layer.

Regarding claim 26, Deml discloses at least one deep trench penetrating through the doped semiconductor layer and extending into the second doped layer.

Regarding claims 28 and 40, Deml discloses a conductive layer 260 and a second insulating layer 250 where the second insulating layer extending at least partly over the shallow

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trench (as in claim 40) being disposed on the charge storing layer and the conductive layer is disposed on the second insulating layer.

Regarding claims 29 and 32, Deml discloses a shallow trench (top wider portion of region 215) containing insulating material (as in claim 32) that is arranged in the doped that is arranged in the doped semiconductor layer.

Regarding claim 30, Deml discloses the shallow trench does not penetrate through the charge storing layer and the insulating layer and the shallow trench extends about laterally symmetrical in all directions beyond an edge of the deep trench.

Regarding claim 31, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 34, Deml discloses at least one shallow trench through which no deep trench penetrates.

Regarding claim 41, Deml discloses a second charge storing layer 260'' disposed on the charge storing layer and the deep trench does not penetrate into the second charge storing layer.

Regarding claim 42, Deml discloses in fig. 16C (see the recessed portion above region 260'') an opening in the second charge storing layer above the deep trench.

Regarding claim 43, Deml discloses edges of the opening are a smaller distance apart than the lateral edges of the deep trench.

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Regarding claim 44, Deml discloses an insulating material that fills the deep trench.

Regarding claims 45 and 46, Deml discloses insulating material or silicon dioxide (as in claim 46) disposed on the wall of the trench.

Regarding claim 49, Deml discloses a plurality of deep trenches each deep trench arranged next to one another in a transverse direction separating a plurality of charge storing layers arranged in the transverse direction.

Regarding claims 50 and 51, Deml discloses a plurality of deep trenches separate a plurality of memory cells forming EEPROM memory cells (as in claim 51) arranged in the transverse direction, the combination of which forms a memory circuit.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gratz in view of Lam et al. ("Lam") USPN 5,545,583.

Gratz discloses the device structure as recited in the claim but lacks anticipation of a shallow trench containing an insulating material.

Lam discloses in figs. 1-4 a device structure circuit arrangement including a shallow trench 40 containing an insulating material or polycrystalline silicon 42 (as in claim 33).

Since Gratz and Lam are both from the same field of endeavor, memory device,

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Lam's teachings would have been recognized in Gratz's pertinent art. Therefore, in view of Lam's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Gratz's device by incorporating an insulating material filled shallow trench since that would minimize unwanted activation and interference with an active wordline as taught by Lam.

14. Claim 36, as understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Gratz in view of Choi et al. ("Choi") KR 2003002709.

Gratz discloses the device structure as recited in the claim but lacks anticipation of deep and shallow trenches of the same depth.

Choi discloses (see abstract) a device structure including a memory circuit arrangement comprising deep and shallow trenches of the same depth.

Since Gratz and Choi are both from the same field of endeavor, memory device, Choi's teachings would have been recognized in Gratz's pertinent art. Therefore, in view of Choi's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Gratz's device by incorporating a deep and shallow trenches of the same depth since that would minimize leakage as taught by Choi.

15. Claims 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gratz in view of Lee ("Lee") US PG-Pub 2002/0058381.

Gratz discloses the device structure including a memory circuit arrangement (as recited in claim 38) but lacks anticipation of a deep trench penetrating through a bottom of the shallow trench.

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Lee discloses in figs. 2A-2O a semiconductor circuit arrangement forming including a deep trench 5 penetrating through a bottom of the shallow trench 3 (see plug 14 penetrating shallow trench 3 in fig. 2O).

Therefore, in view of Lee's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Gratz's device by incorporating a deep trench penetrating through a bottom of a shallow trench since that would minimize the size of the memory device as taught by Lee.

Regarding claim 39, as understood, Lee discloses an electrically conductive layer 14 extends partly over the shallow trench.


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
May 4, 2005